A 1.5GHz Third Generation Itanium® Processor

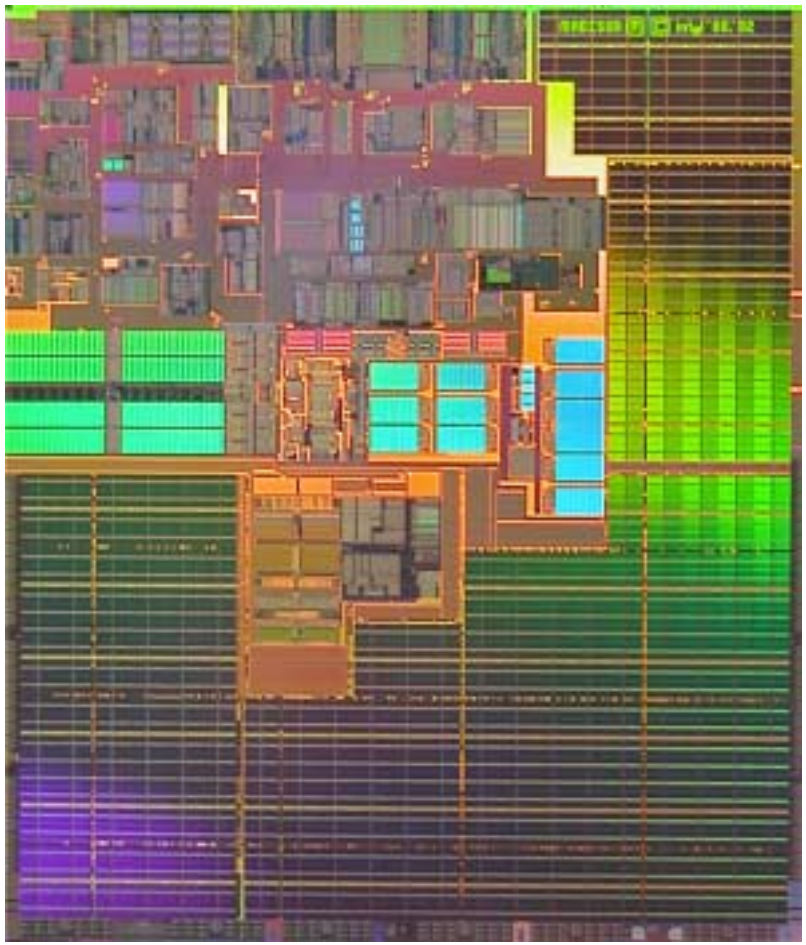
Jason Stinson, Stefan Rusu

Intel Corporation, Santa Clara, CA

Outline

- Processor highlights
- Process technology details
- Itanium® processor evolution
- Block diagram
- Cache circuit design details
- Package details
- Front-side bus interface
- Clock distribution
- Power dissipation
- RAS, DFT and DFM features
- Frequency shmoo
- Summary

130nm Itanium® 2 Processor Highlights

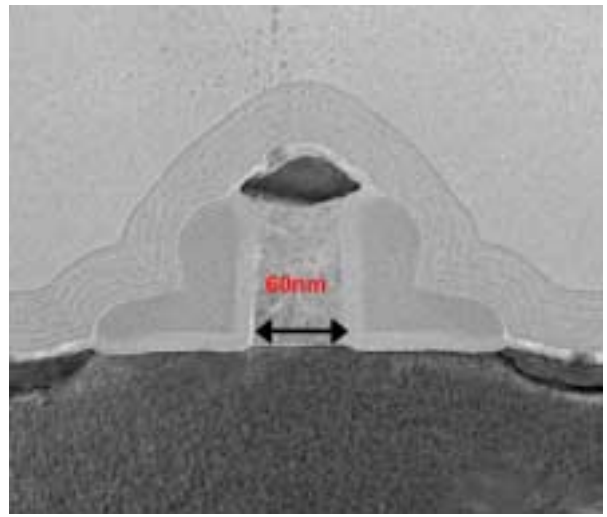


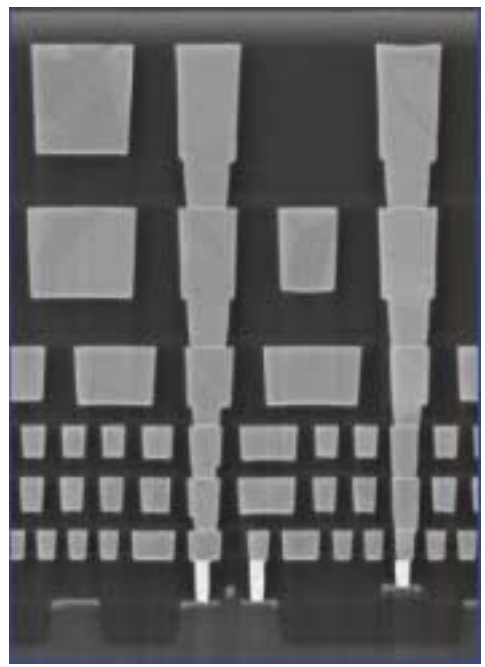
- 410M transistors
- 374mm^2 die size
- 6MB on-die L3 cache
- 1.5GHz at 1.3V
- 6.4GB/s 400MT/s 4-way bus interface
- Plug-in compatible with existing platforms
- Extensive RAS, DFT and DFM features

Largest microprocessor transistor count and on-die cache

130nm Process Characteristics

Attribute	Value
Lgate	60nm
M1 pitch	350nm
M2 pitch	448nm
M3 pitch	448nm
M4 pitch	756nm
M5 pitch	1120nm
M6 pitch	1204nm
Dielectric	FSG, K=3.6
Memory cell	2.45µm^2





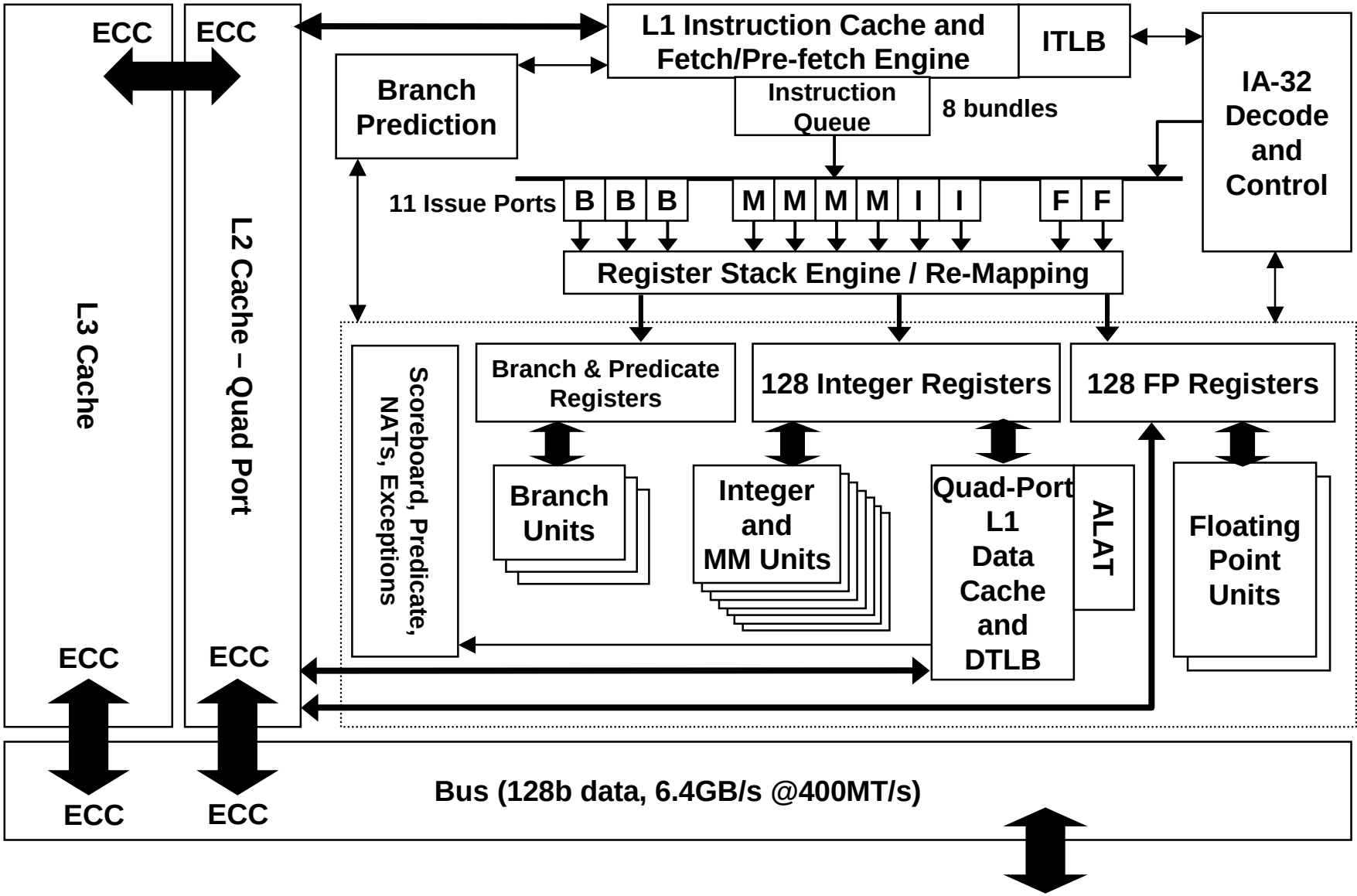
S. Thompson et al, IEDM 2001 (top)
S. Tyagi, et al, IEDM 2000 (bottom)

Itanium® Processor Evolution

Attribute	Itanium® Processor	Itanium® 2 Processor	This work
Architecture	Explicitly Parallel Instruction Computing		
Process	180nm	180nm	130nm
Device Count	25M	221M	410M
On-die L3 cache	0*	3MB	6MB
Frequency	800MHz	1.0GHz	1.5GHz
Supply Voltage	1.6V	1.5V	1.3V
Power	130W*	130W	130W

* Includes 4MB cache on cartridge

Block Diagram

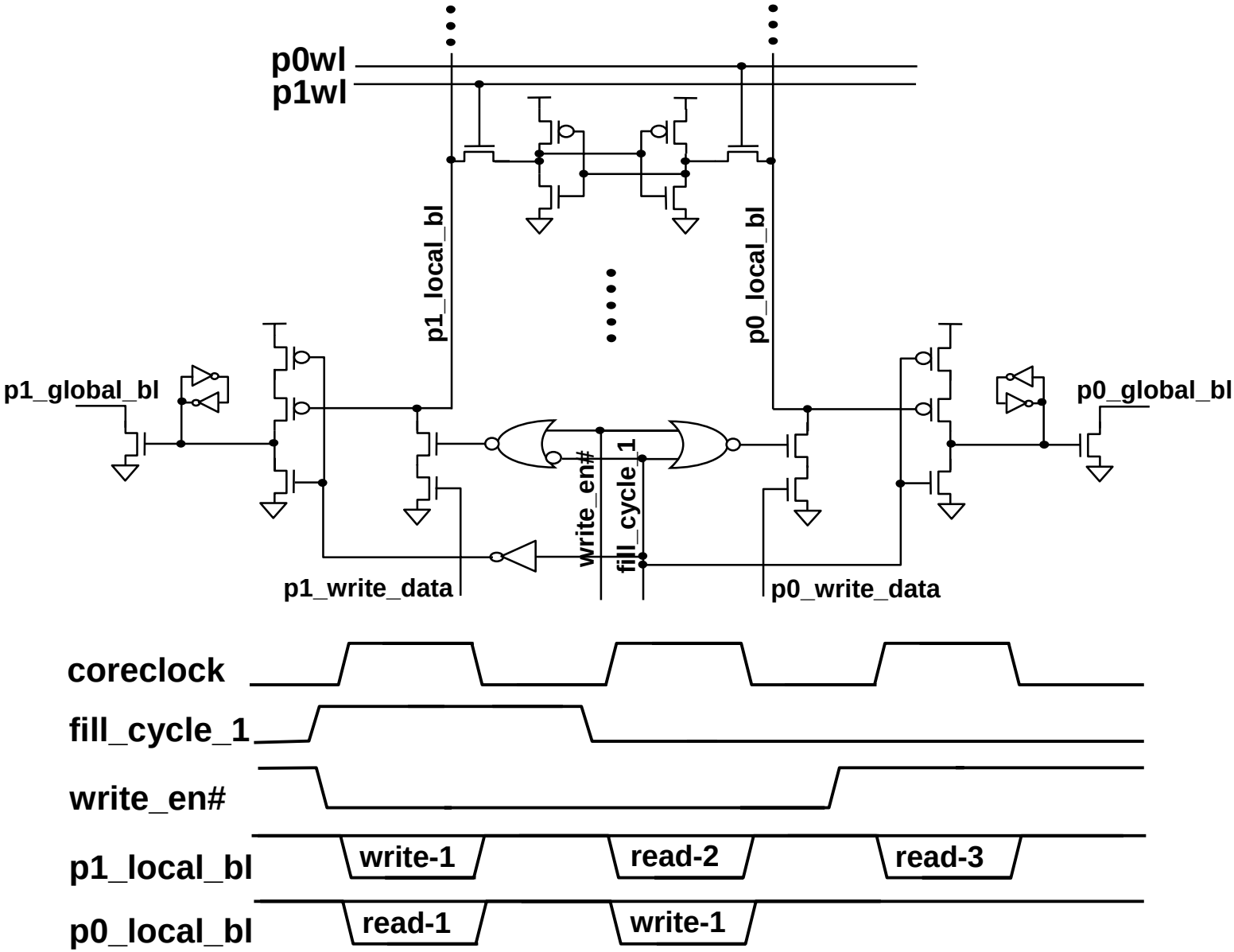


Cache Summary

Attribute	L1I	L1D	L2	L3
Size	16K	16K	256K	6M
Line Size	64B	64B	128B	128B
Ways	4	4	8	24
Replacement	LRU	NRU	NRU	NRU
Latency	1-Fetch:1	INT:1 FP: NA	INT: 5 FP: 6	14
Write Policy	-	WT (RA)	WB (WA)	WB (WA)
Bandwidth	R: 48GBs	R: 24GBs W: 24GBs	R: 48GBs W: 48GBs	R: 48GBs W: 48GBs

- Cache bandwidth increased by 50%
- L3 cache latency increased to 14 clocks and set associativity doubled

L1 Instruction Cache Circuit Detail



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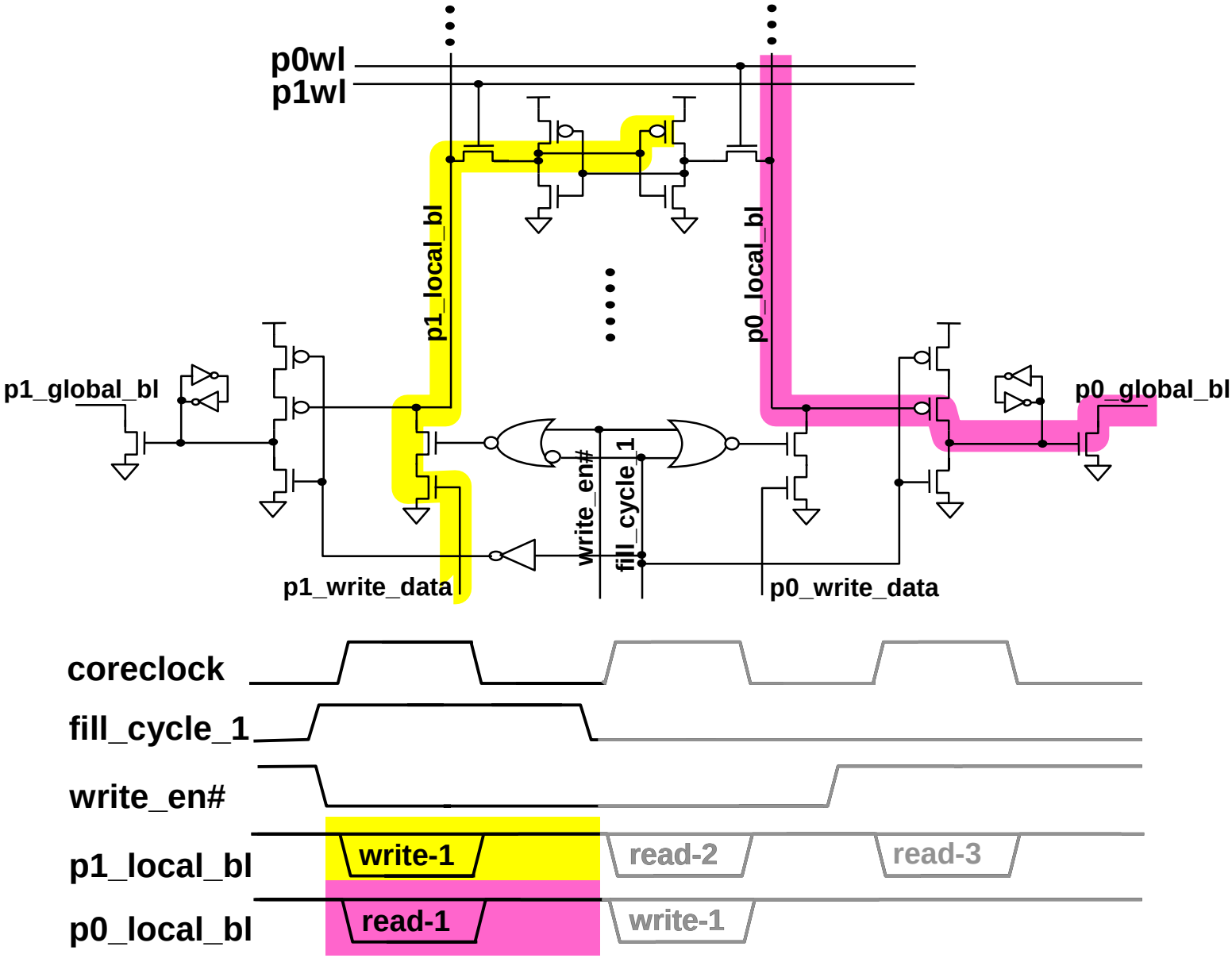
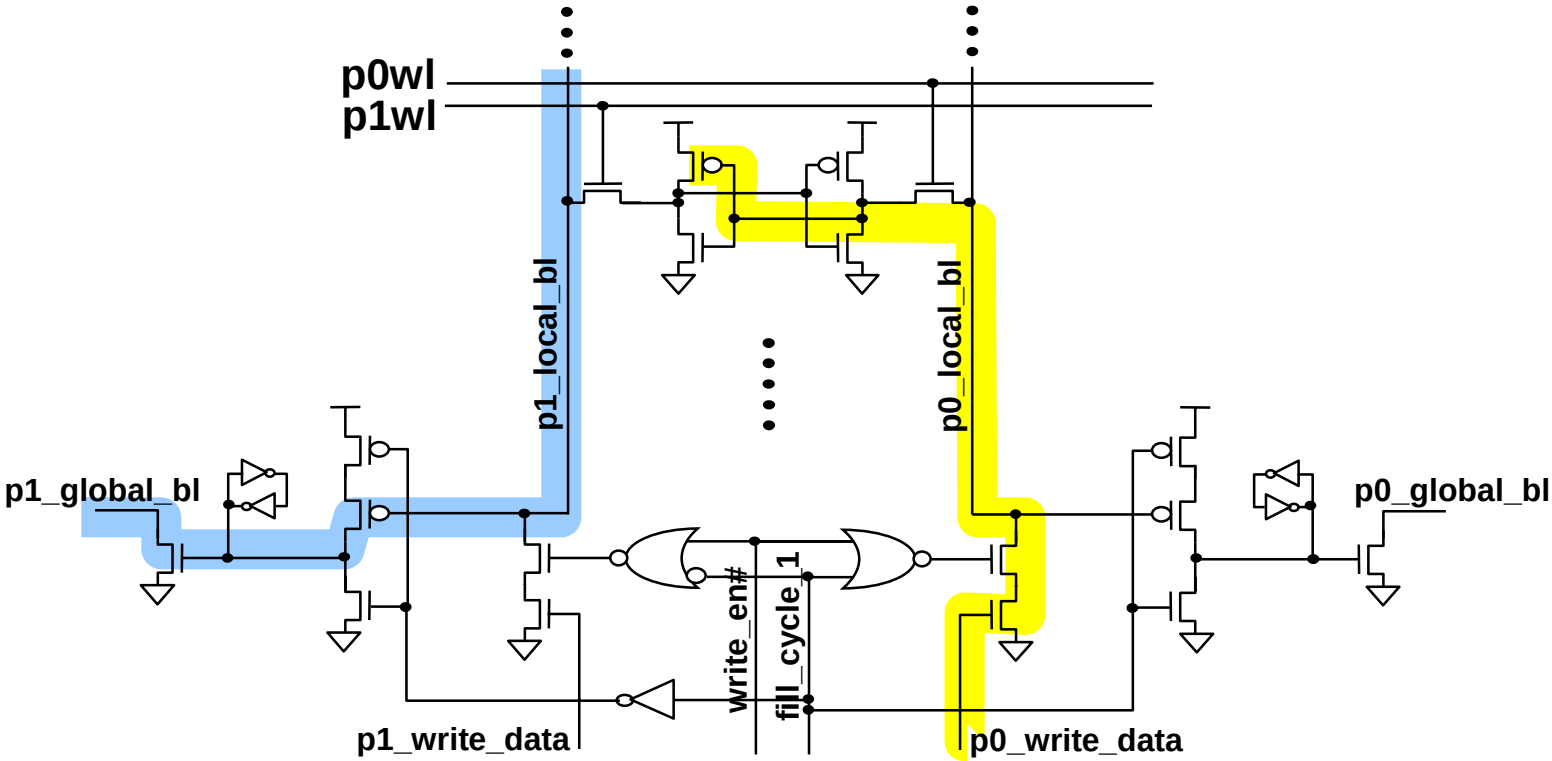
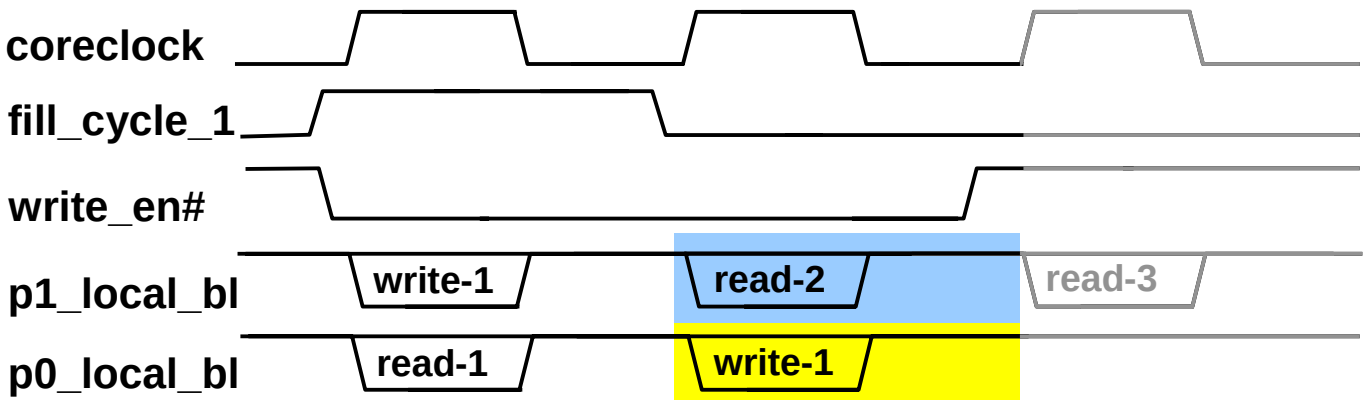
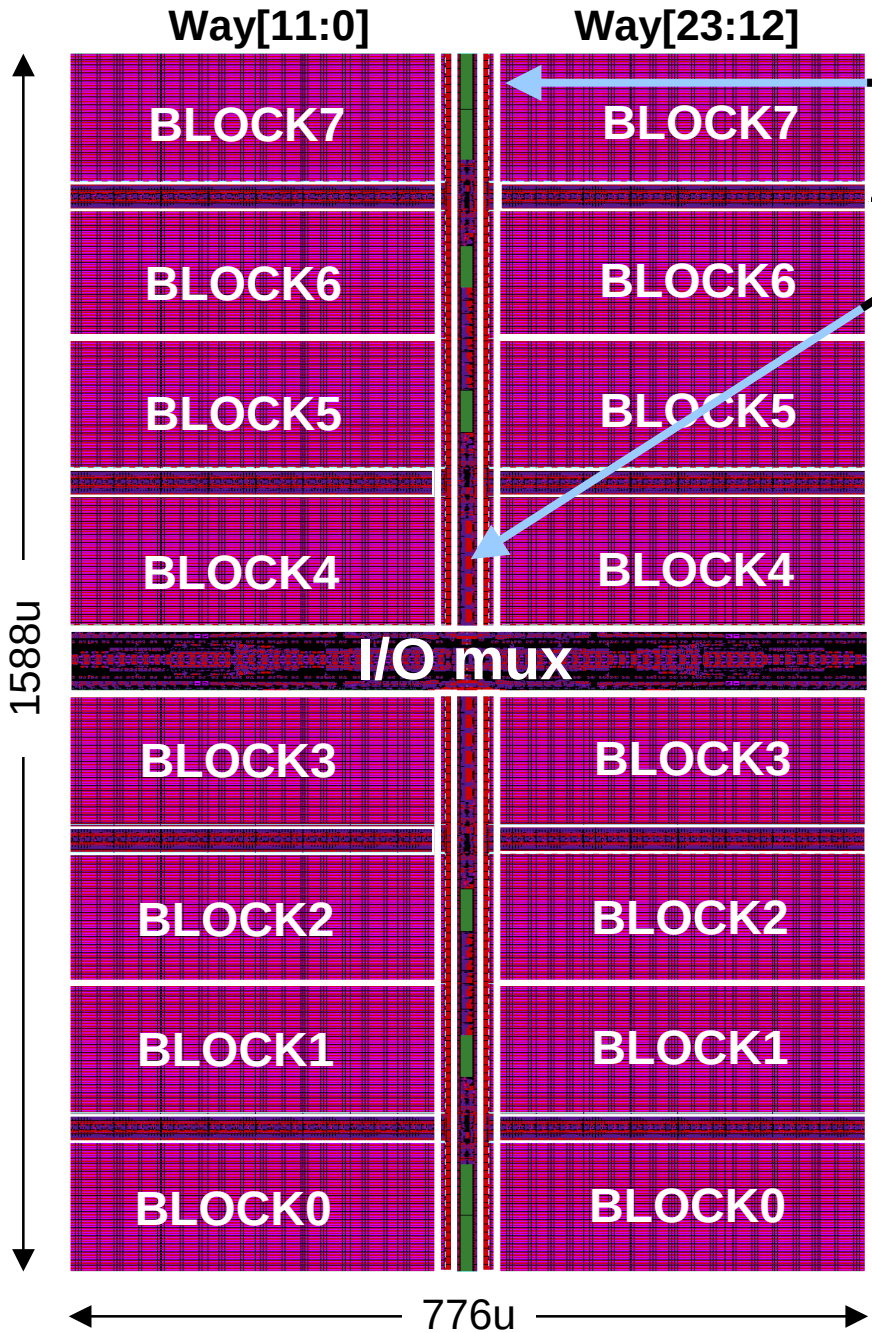


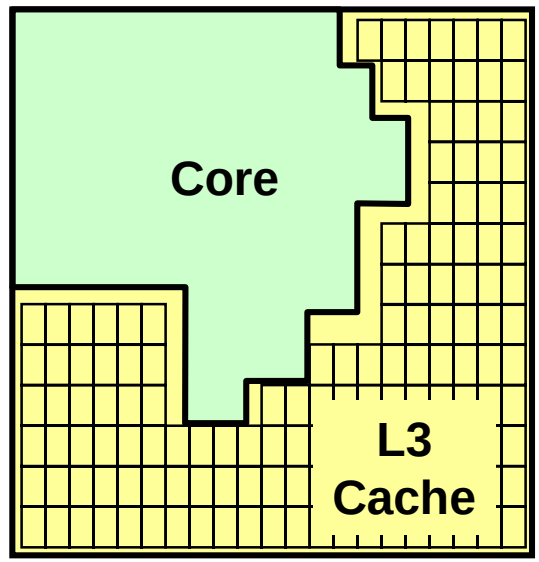
L1 Instruction Cache Circuit Detail





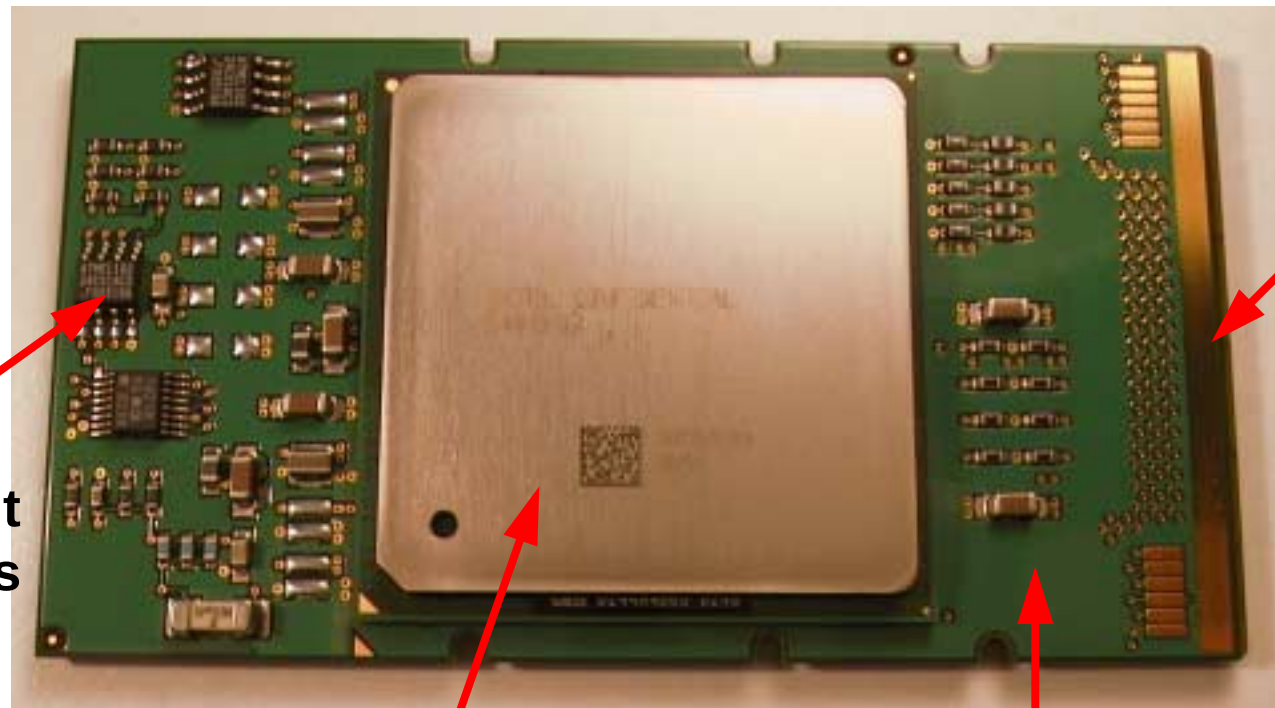
L3 Subarray





- L3 cache contains 140 subarrays tiled to fit irregular shape of core

Package Details



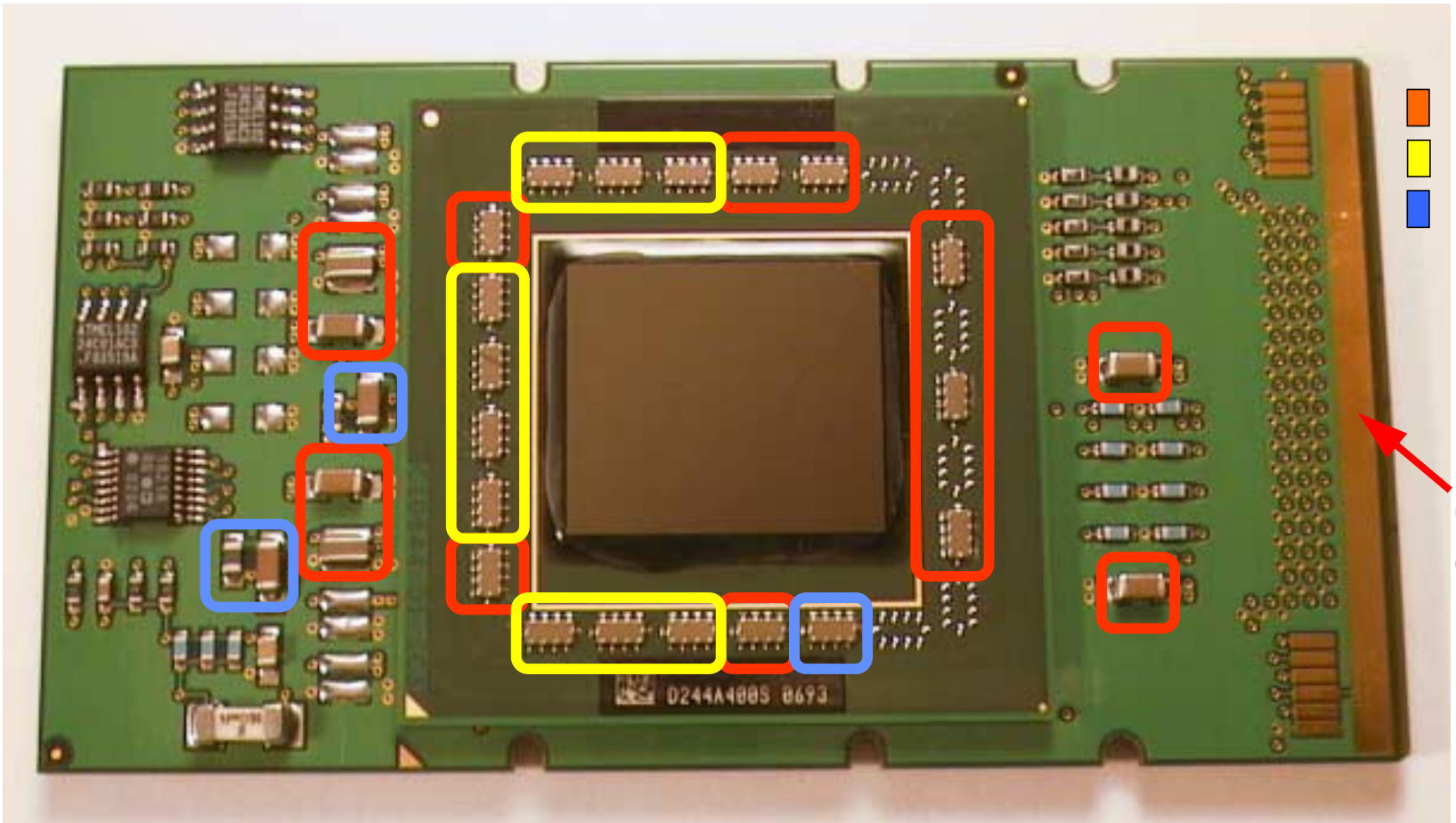
Server Management Components

Power delivery connector

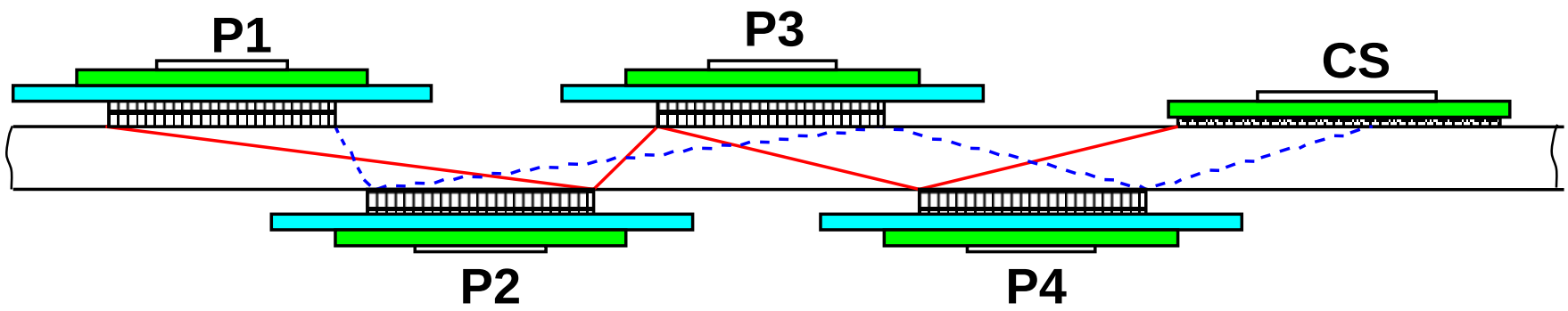
Flip-Chip BGA package with Integrated Heat Spreader

Interposer Substrate

Package Decoupling

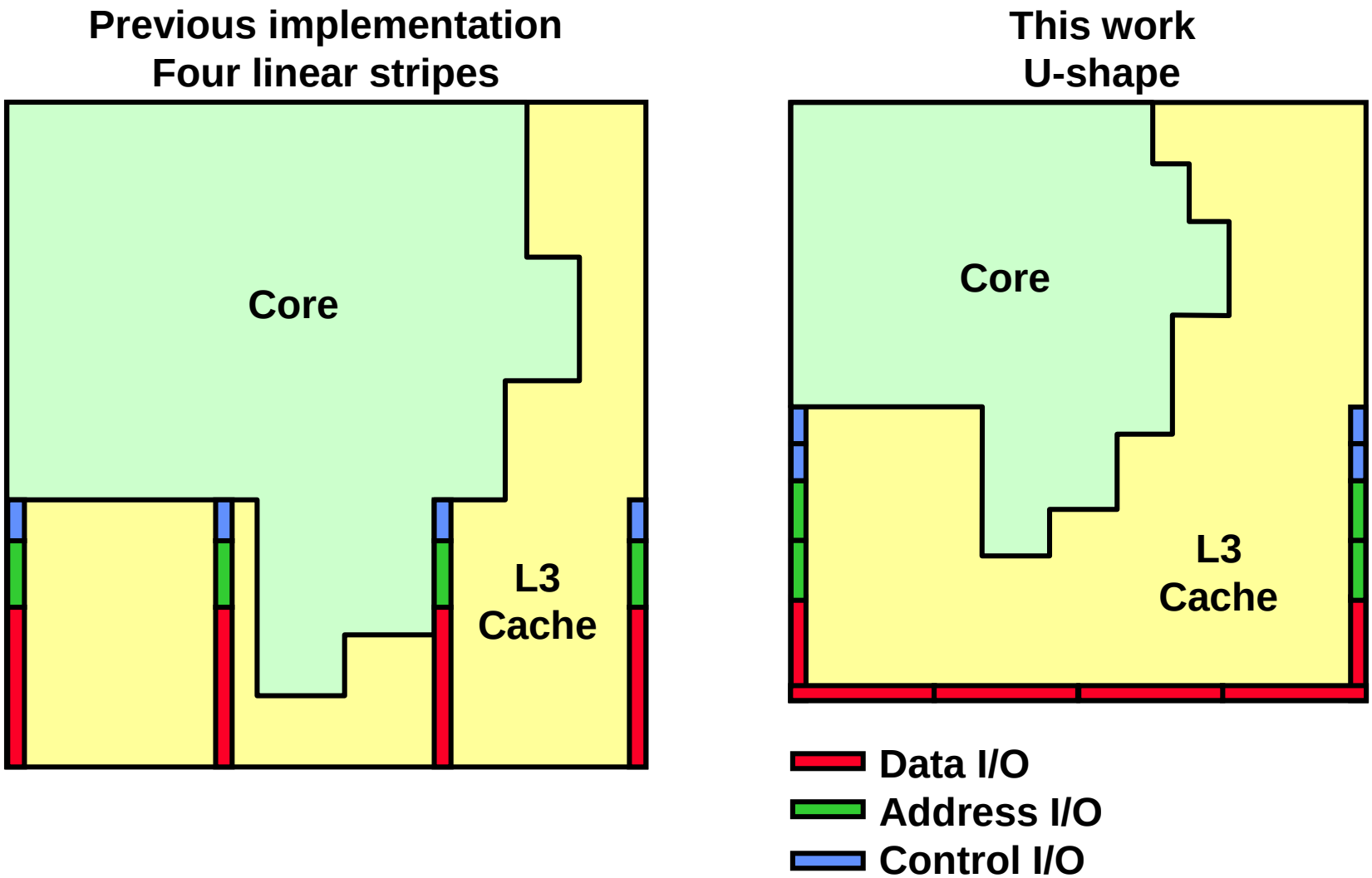


Front Side Bus



Interface Support	Glueless 4-way Multi-Processor
System Topology	Dual-sided board, staggered vias
Termination Voltage	1.2V, common ground with core
Voltage Reference	Ground-referenced, 0.75V Vref
Data Bus Width	128-bit
Data Bus Speed	400MT/s source synchronous
Data Strobes	1 differential strobe for 16b of data
Peak BW	6.4GB/s
Address, Control Speed	200MHz common clock

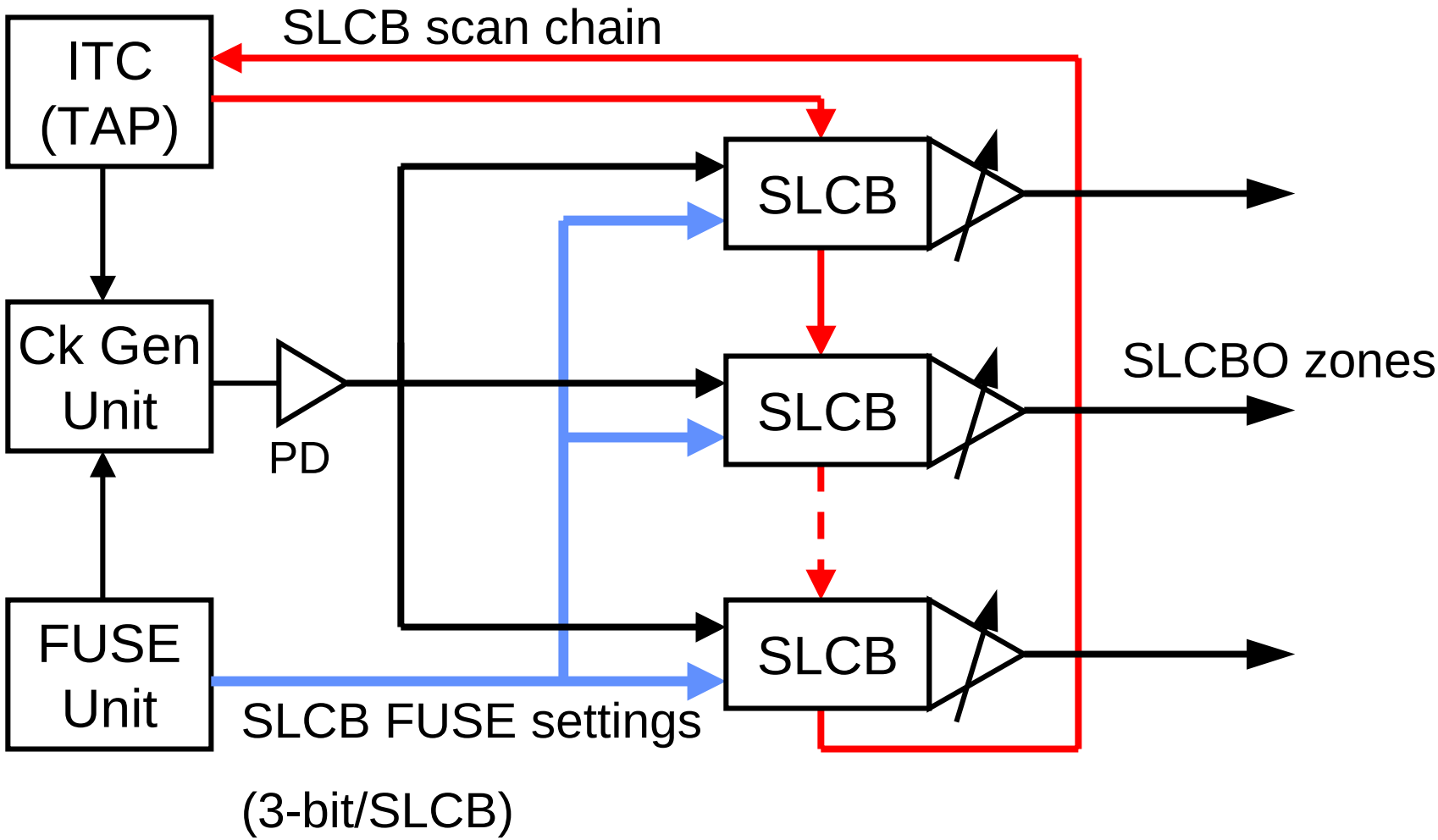
Front-Side Bus Topology



Itanium® Processor Clock Distribution Trends

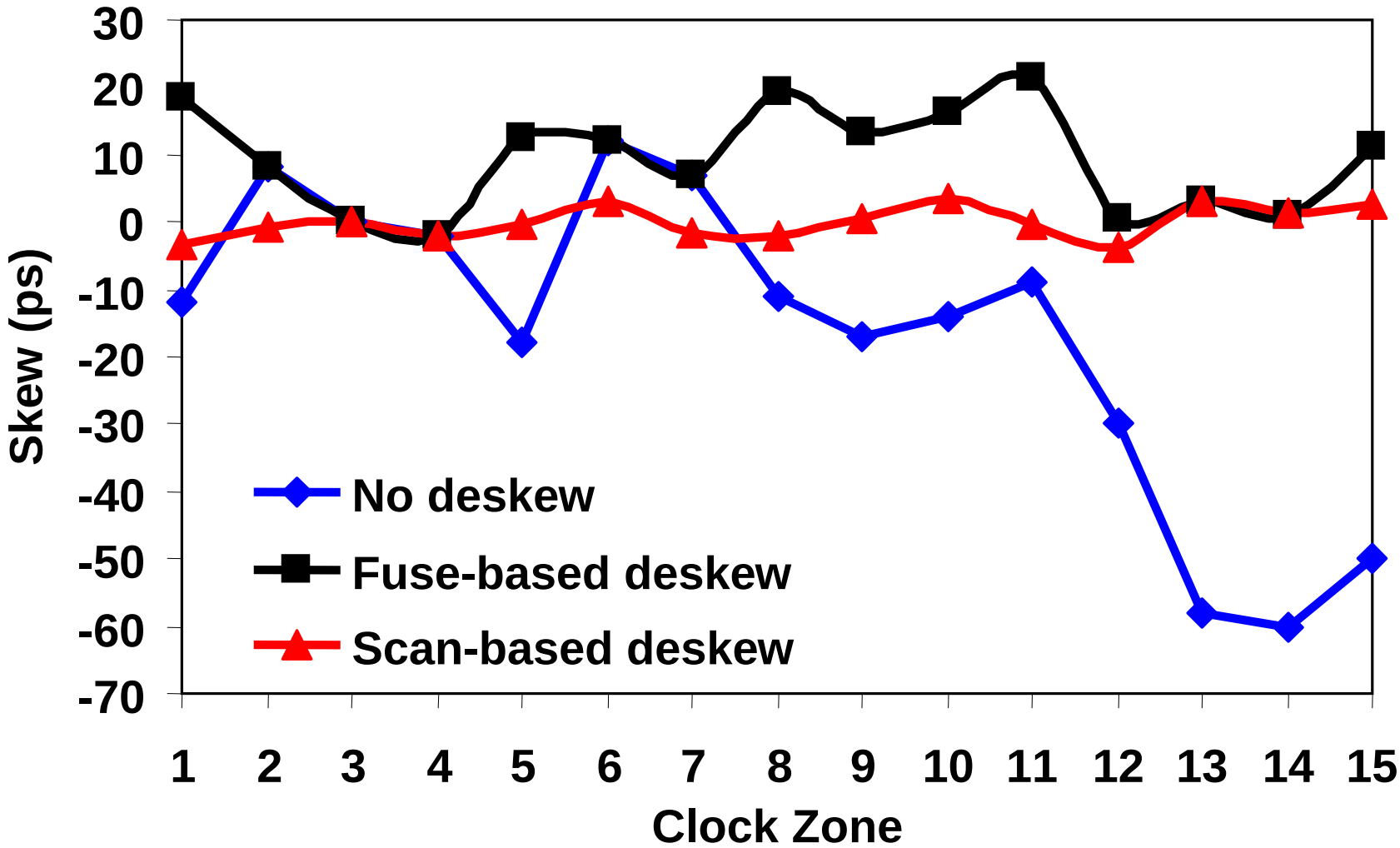
Attribute	Itanium® Processor	Itanium® 2 Processor	This work
Process/Metal	180nm / Al	180nm / Al	130nm / Cu
Primary tree	Single ended	Differential	Differential
Local distribution	Grid	Tree	Tree
Clock skew [ps]	28ps	62ps	24ps
Deskew Method	Active	On-demand	Fuse-based

Fuse-Based Clock Deskew



SLCB = Second Level Clock Buffer

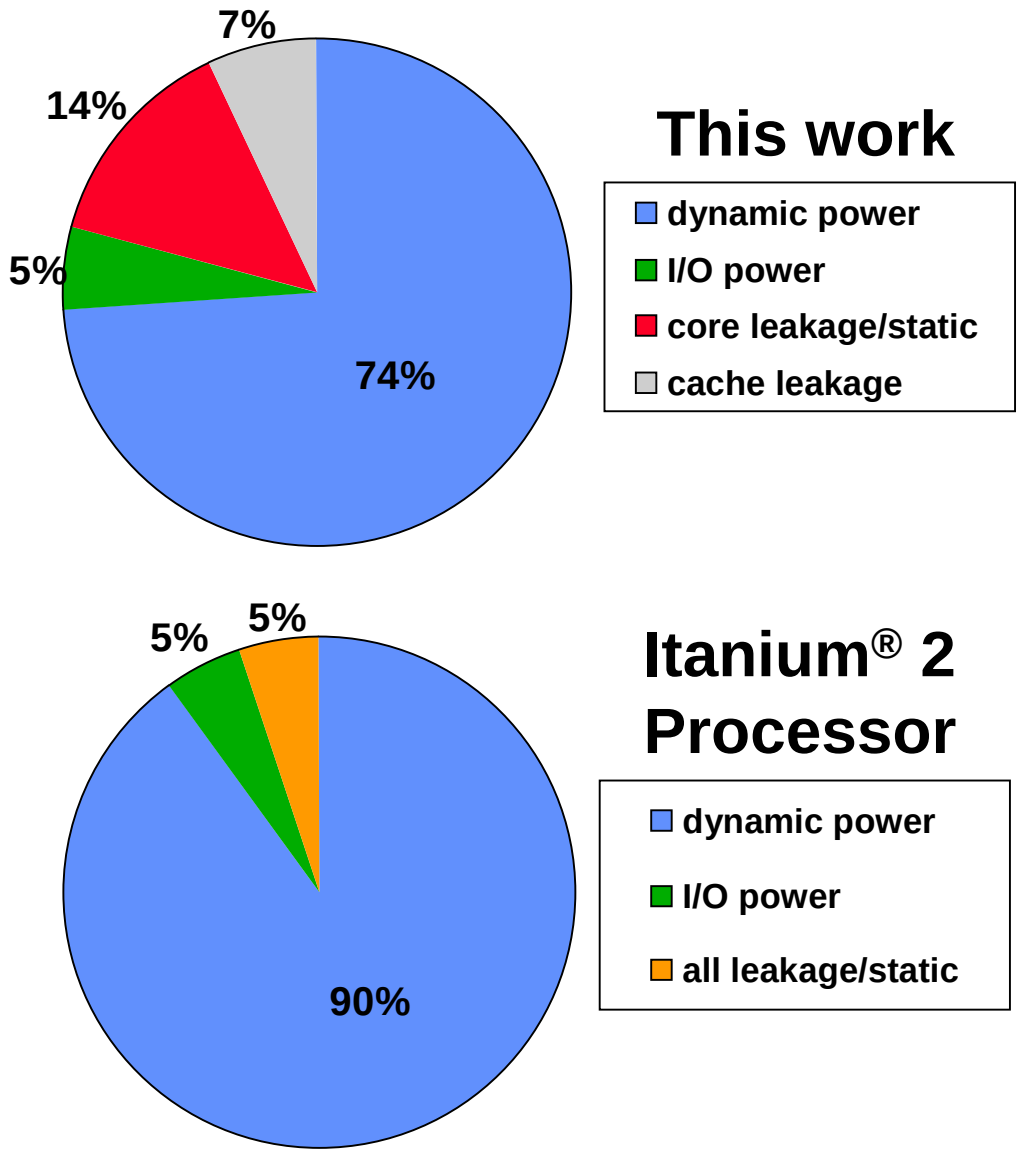
Clock Zone Skew Plot



- Worst case clock skew is 24ps in fuse mode and 7ps in scan mode

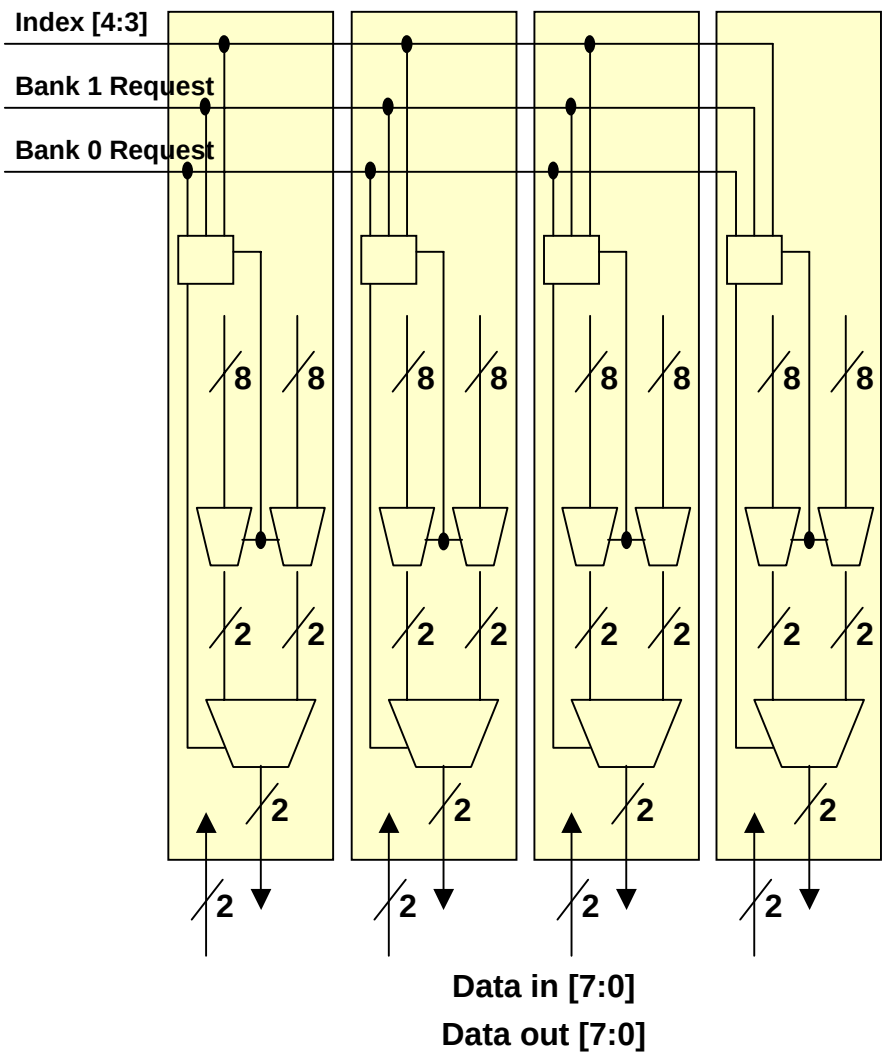
Power

- **Same 130W power envelope as the 0.18um Itanium® 2 processor**
  - **50% frequency increase**
  - **2X larger L3 cache**
  - **Leakage increased 3.5X**
- **Aggressive management of dynamic power**
  - **Reduced clock loading**
  - **Reduced contention power**
  - **L3 cache power management**



L3D Power Reduction Scheme

Previous Implementation



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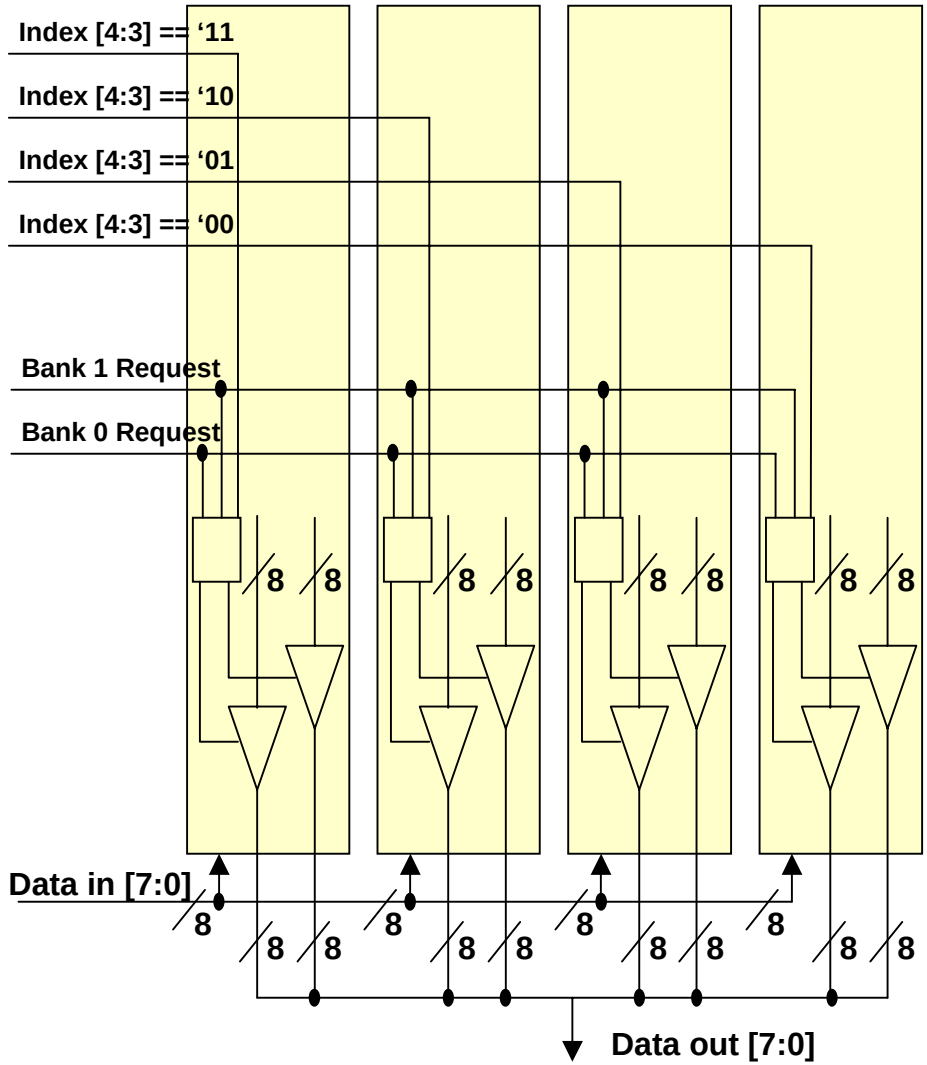
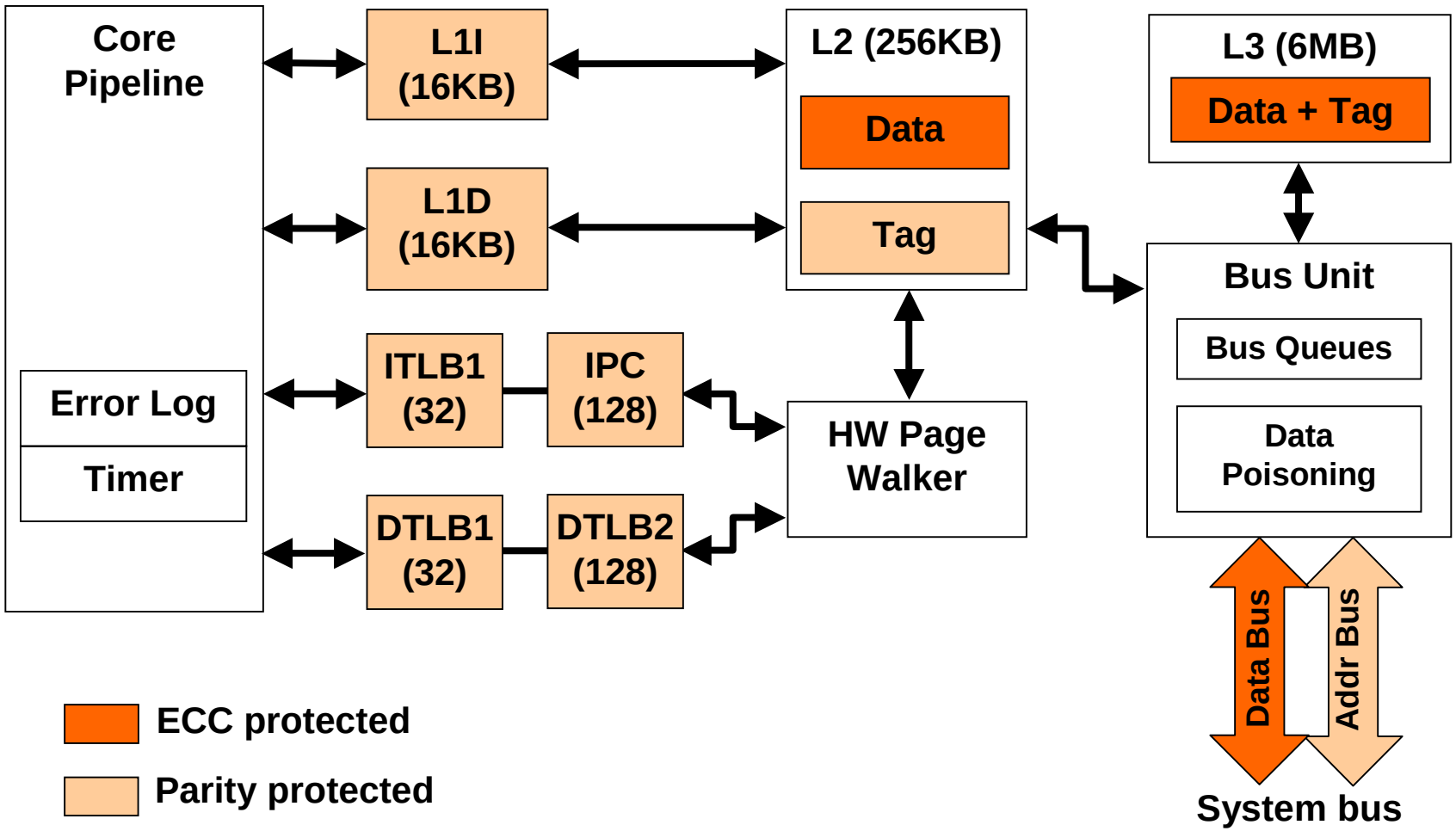


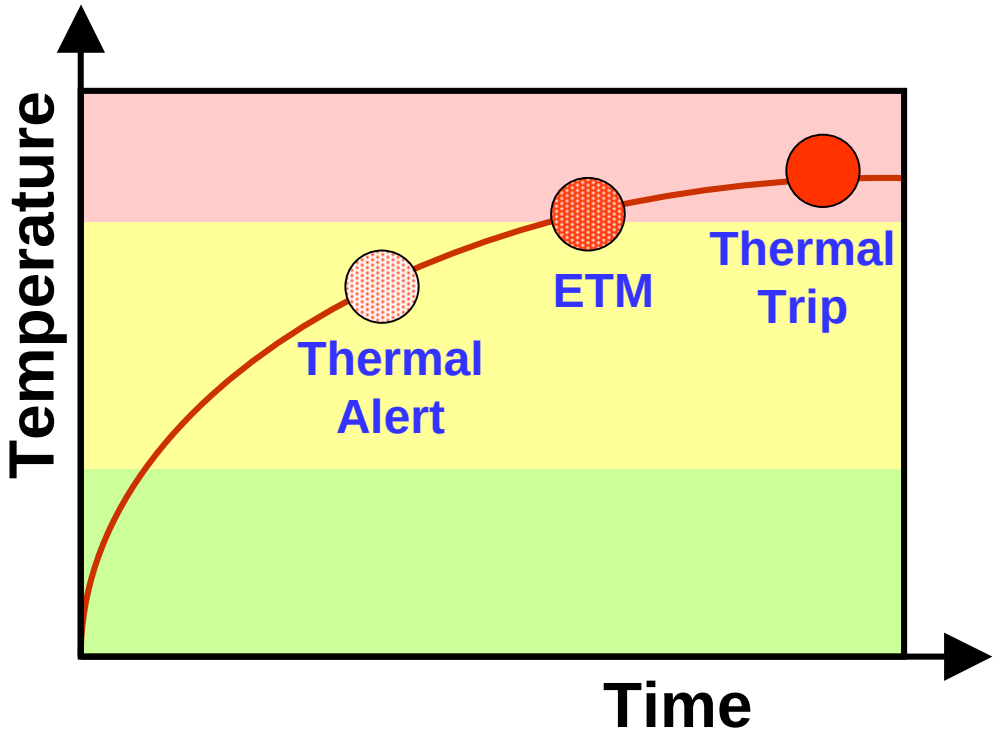
Reliability Features

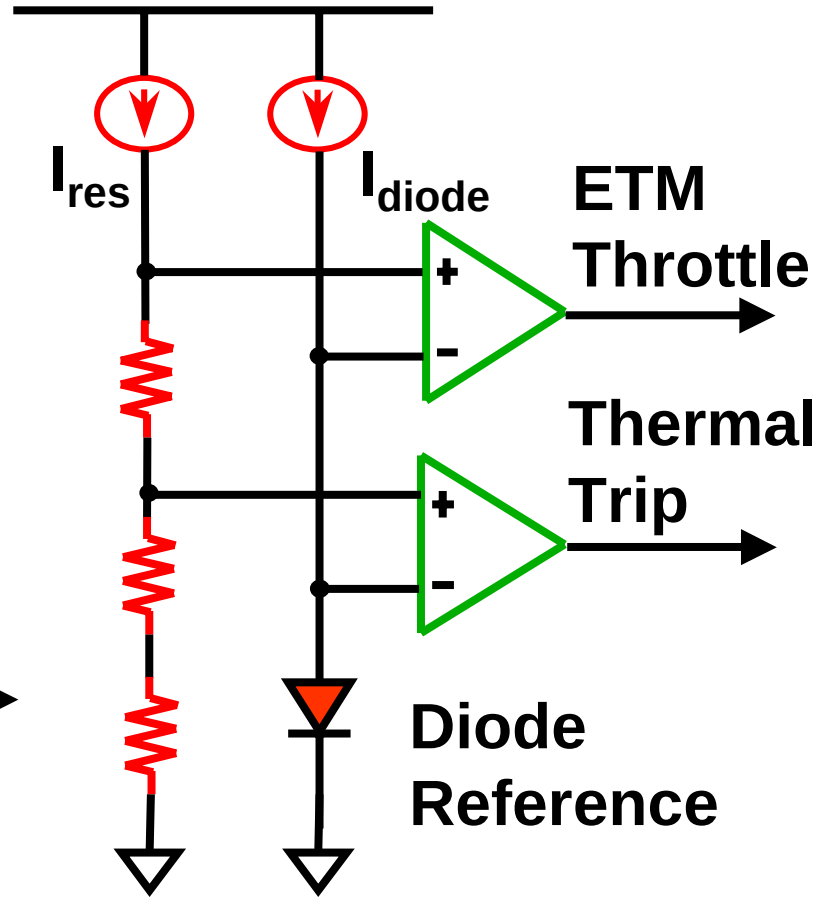


DFT/DFM Feature Summary

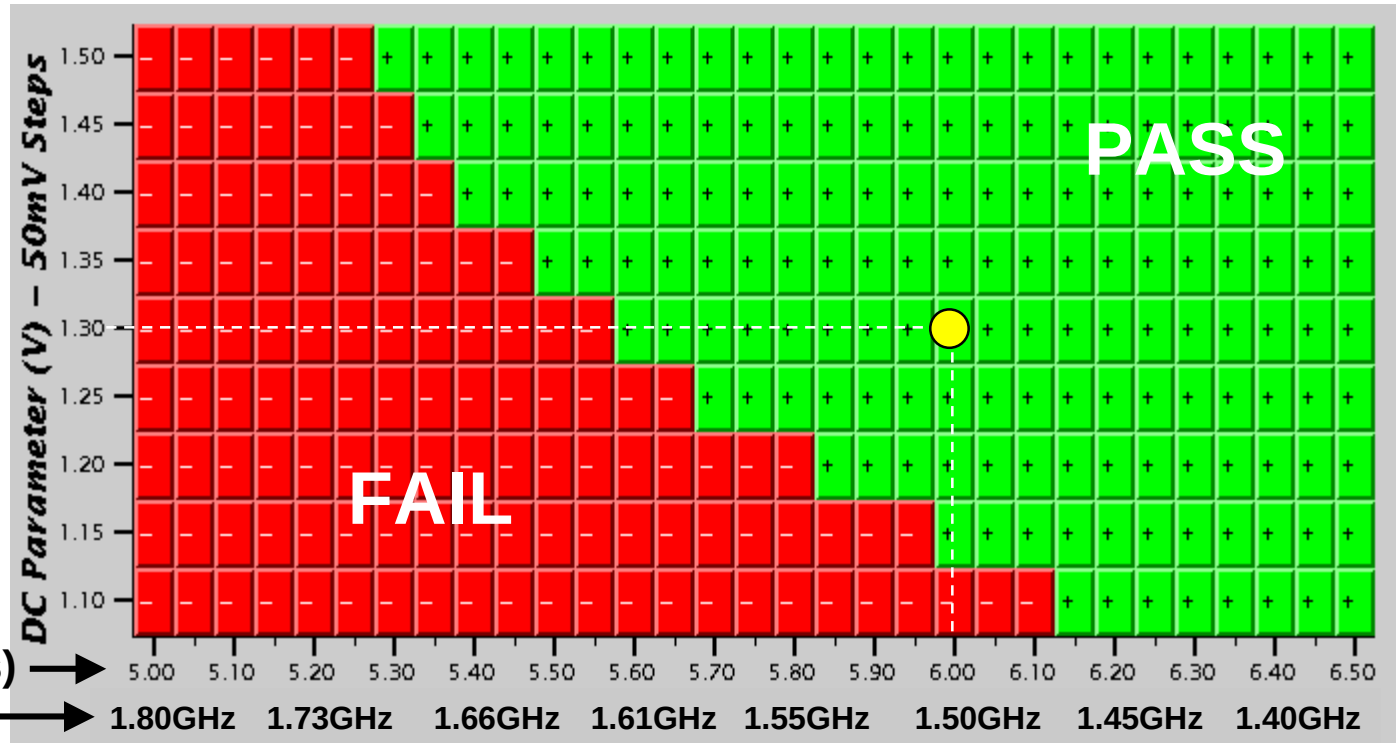
Feature	Itanium® Processor	Itanium® 2 Processor	This work
Scan Coverage	48K	140K	140K
Scanout Coverage	5.5K	24K	24K
Cache DAT Mode (major arrays)	Yes	Yes	Yes
L3 Redundancy / Repair	N/A	Dual	Quad
Weak-Write Test Mode	Fixed	Fixed	Programmable
IO DFT	Basic IO Loopback	Limited IO Loopback	Enhanced IO Loopback
Dynamic Frequency Adjustment	Multi-cycle shrink/stretch	Single cycle shrink/stretch	Multi-cycle shrink/stretch
On-die process monitors	No	No	Yes

Thermal Protection Features





Frequency Shmoo



Frequency increased by 50% from previous generation

Summary

- **The 2003 version of the Itanium® 2 processor (Madison) delivers 2X larger on-die cache and 50% increase in frequency**
- **Compatible with today's Itanium® 2-based systems**
- **Enterprise-class RAS, DFT and DFM features**
- **Largest on-die cache and transistor count ever reported for a microprocessor**
- **6.4GB/s multi-drop bus interface**
- **Clock de-skew technique achieves 24ps skew in fuse-mode and 7ps in scan mode across entire die**